

## CLAIMS

What is claimed is:

- 1    1.     A power amplifier comprising:  
2    a first switching device connected between a first supply voltage and a first output node;  
3    a second switching device connected between a second supply voltage and a second  
4        output node; and  
5    an inductance coupled between the first and second output nodes.
- 1    2.     The power amplifier of claim 1, wherein a load is coupled to the second output  
2    node.
- 1    3.     The power amplifier of claim 1, further comprising a first capacitor coupled to the  
2    first output node, and a second capacitor coupled to the second output node.
- 1    4.     The power amplifier of claim 1, further comprising a first capacitor coupled to the  
2    first output node.
- 1    5.     The power amplifier of claim 1, further comprising a first capacitor coupled  
2    between the first and second output nodes.
- 1    6.     The power amplifier of claim 1, wherein the first and second switching devices  
2    are driven by signals that repeatedly turn the devices on and off.

1 7. The power amplifier of claim 6, wherein the first and second switching devices  
2 are both cycled on during the same time period, and wherein the first and second  
3 switching devices are both cycled off during the same time period.

1 8. The power amplifier of claim 4, wherein the first capacitor is provided by the  
2 input capacitance of a third switching device.

1 9. The power amplifier of claim 3, wherein the first capacitor is provided by the  
2 input capacitance of a third switching device, and wherein the second capacitor is  
3 provided by the input capacitance of a fourth switching device.

1 10. The power amplifier of claim 1, wherein the first and second switching devices  
2 are comprised of transistors.

1 11. The power amplifier of claim 1, wherein the first switching device is comprised of  
2 a PMOS transistor, and wherein the second switching device is comprised of an NMOS  
3 transistor.

1 12. The power amplifier of claim 1, further comprising a load coupled across the first  
2 and second output nodes.

1 13. The power amplifier of claim 1, further comprising a transformation network  
2 coupled to the first and second output nodes.

1 14. The power amplifier of claim 13, wherein the transformation network further  
2 comprises:  
3 a capacitor coupled to the first output node and a third node;  
4 an inductor coupled to the second output node and the third node; and  
5 a load coupled to the third node.

1 15. The power amplifier of claim 1, further comprising a preamplifier connected to  
2 the power amplifier, the preamplifier further comprising:  
3 a third switching device connected between said first supply voltage and a third node and  
4 coupled to the input to the first switching device;  
5 a fourth switching device connected between said second supply voltage and a fourth  
6 node and coupled to the input to the second switching device; and  
7 a second inductor coupled between the third and fourth nodes.

1 16. The power amplifier of claim 1, further comprising one or more inductors coupled  
2 between the first output node and a third supply voltage.

1 17. The power amplifier of claim 1, further comprising one or more inductors coupled  
2 between the first output node and a third supply voltage, and one or more inductors  
3 coupled between the second output node and a fourth supply voltage.

1 18. A method of reducing the peak output voltage of an amplifier comprising the  
2 steps of:  
3 providing an inductor having first and second terminals;

4 providing a first switching device connected between the first terminal of the inductor  
5 and a first supply voltage;  
6 providing a second switching device connected between the second terminal of the  
7 inductor and a second supply voltage;  
8 applying a voltage between the first and second terminals of the inductor during a first  
9 portion of a clock cycle by turning on the first and second switching devices; and  
10 turning off the first and second switching devices during a second portion of the clock  
11 cycle.

1 19. The method of claim 18, further comprising the steps of providing a first  
2 capacitance connected to the first terminal, providing a second capacitance connected to  
3 the second terminal, wherein current from the inductor charges or discharges the first and  
4 second capacitances during the second portion of the clock cycle.

1 20. The method of claim 18, further comprising the step of connecting a load to the  
2 first node.

1 21. The method of claim 18, wherein the load includes a reactive network.

1 22. The method of claim 18, further comprising the step of driving the first and  
2 second switching devices such that the switching devices are turned on and off  
3 simultaneously.

1 23. The method of claim 18, further comprising the step of driving the first and  
2 second switching devices by repeatedly turning both devices on and then turning both  
3 devices off.

1 24. The method of claim 18, wherein the switching devices are comprised of  
2 transistors.

1 25. The method of claim 18, further comprising the step of differentially connecting a  
2 load to the first and second nodes.

1 26. The method of claim 18, wherein the load is connected across the first and second  
2 nodes.

1 27. The method of claim 18, further comprising the steps of:  
2 providing a third switching device connected between the gate of the first switching  
3 device and a third supply voltage;  
4 providing a fourth switching device connected between the gate of the second switching  
5 device and a fourth supply voltage; and  
6 providing a second inductor connected between the gates of the first and second  
7 switching devices.

1 28. A differential power amplifier comprising:  
2 a first amplifier having a first switching device connected between a first supply voltage  
3 and a first output node, a second switching device connected between a second  
4 supply voltage and a second output node, and an inductance coupled between the  
5 first and second output nodes;  
6 a second amplifier having a third switching device connected between a third supply  
7 voltage and a third output node, a fourth switching device connected between a

8 fourth supply voltage and a fourth output node, and an inductance coupled  
9 between the third and fourth output nodes; and  
10 wherein the first and second amplifiers are coupled together to drive a load.

1 29. The differential power amplifier of claim 28, wherein the second and fourth  
2 output nodes of the first and second amplifiers are coupled together to drive the load.

1 30. The differential power amplifier of claim 28, wherein the first, second, third, and  
2 fourth output nodes of the first and second amplifiers are coupled together to drive the  
3 load.

1 31. The differential power amplifier of claim 28, further comprising:  
2 a first transformation network connected between the first and second output nodes of the  
3 first amplifier and the load, and  
4 a second transformation network connected between the third and fourth output nodes of  
5 the second amplifier and the load.

1 32. The differential power amplifier of claim 28, further comprising:  
2 a first transformation network connected between the second output node of the first  
3 amplifier and the load, and  
4 a second transformation network connected between the third output node of the second  
5 amplifier and the load.

1 33. The differential power amplifier of claim 28 further comprising:  
2 an inductor coupled between the first output node and the third output node.

1 34. The differential power amplifier of claim 28 further comprising:  
2 an inductor coupled between the second output node and the fourth output node.

1 35. The differential power amplifier of claim 31, wherein the first transformation  
2 network further comprises:  
3 a first capacitor coupled to the second output node of the first amplifier and coupled to  
4 the load; and  
5 a first inductor coupled to the first output node of the first amplifier and coupled to the  
6 load.

1 36. The differential power amplifier of claim 31, wherein the second transformation  
2 network further comprises:  
3 a second capacitor coupled to the third output node of the second amplifier and coupled  
4 to the load; and  
5 a second inductor coupled to the fourth output node of the second amplifier and coupled  
6 to the load.

1 37. The differential power amplifier of claim 28, wherein the first amplifier receives  
2 first and second inputs.

1 38. The differential power amplifier of claim 37, wherein the first and second  
2 switching devices of the first amplifier are enabled and disabled simultaneously; and  
3 wherein the third and fourth switching devices of the second amplifier are enabled and  
4 disabled simultaneously.

1 39. The differential power amplifier of claim 38, wherein the first and second  
2 switching devices of the first amplifier are enabled during the time that the third and  
3 fourth switching devices of the second amplifier are disabled, and wherein the third and  
4 fourth switching devices of the second amplifier are enabled during the time that the first  
5 and second switching devices of the first amplifier are disabled.

1 40. The differential power amplifier of claim 28, wherein the amplifier further  
2 comprises:  
3 a first capacitance coupled between the first output node and the first supply voltage;  
4 a second capacitance coupled between the second output node and the first supply  
5 voltage; and  
6 wherein the second amplifier further comprises:  
7 a third capacitance coupled between the third output node and a third supply voltage;  
8 a fourth capacitance coupled between the fourth output node and a fourth supply  
9 voltage.

1 41. The differential power amplifier of claim 40, wherein the first, second, third, and  
2 fourth capacitances are provided by capacitors.

1 42. The differential power amplifier of claim 40 wherein the first, second, third, and  
2 fourth capacitances are provided by the input capacitance of fifth, sixth, seventh, and  
3 eighth switching devices, respectively.

1 43. The differential power amplifier of claim 42, wherein the fifth switching device is  
2 coupled to the third output node, and the sixth switching device is coupled to the fourth



3 output node, and the seventh switching device is coupled to the first output node, and the  
4 eighth switching device is coupled to the second output node.

1 44. The differential power amplifier of claim 28, further comprising a preamplifier for  
2 each of the first and second power amplifiers.

1 45. The differential power amplifier of claim 44, wherein each of the preamplifiers  
2 further comprise:  
3 fifth and sixth switching devices connected between the first and second supply voltages;  
4 and  
5 a third inductor connected between the fifth and sixth switching devices.

1 46. The differential power amplifier of claim 28, wherein the first and second  
2 amplifiers are cross-coupled.